APPLICATIONS OF A DIFFERENTIAL LATCH

ABSTRACT OF THE DISCLOSURE

A differential latch includes a sample transistor section, a hold transistor section, a 1st gating circuit and a 2nd gating circuit. The sample transistor section is operably coupled to sample, when coupled to a supply voltage (e.g., V_{DD} and V_{SS}) a differential input signal. The hold transistor section is operably coupled to latch, when coupled to the supply voltage, the sampled differential input to produce a latched differential signal. The 1st gating circuit is operable to couple the sampled transistor section to the supply voltage in accordance with a 1st clocking logic operation and a 2nd clocking logic operation. The 2nd gating circuit is operable to couple the hold transistor section to the supply voltage in accordance with a 3rd clocking logic operation and a 4th clocking logic operation.